UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/633,899	08/04/2003	Brian D. McMinn	5500-90000	5825

7590 09/13/2005

Lawrence J. Merkel
Meyertons, Hood, Kivlin, Kowert & Goetzel, P.C.
P.O. Box 398
Austin, TX 78767

EXAMINER	
ELLIS, KEVIN L	

ART UNIT	PAPER NUMBER
2188	

DATE MAILED: 09/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/633,899	MCMINN ET AL.	
	Examiner	Art Unit	
	Kevin L. Ellis	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-17 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-17 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 12/15/03.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Detailed Action

1. Claims 1-17 are presented for examination.

2. Information disclosed and listed on PTO 1449 has been considered.

Claim Rejections – 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

4. Claims 1-9 are rejected under 35 U.S.C. § 102(e) as being anticipated by Clift et al., U.S. Patent 6,633,970.

A) As to claims 1, 2, and 6, Clift et al. discloses the invention as claimed. There is a mapper circuit that provides associations between logical registers and physical registers (see Abstract, Fig 2-5), the mapper circuit comprising a memory that has a plurality of addressable units addressed by different logical register names (LRN) that stores a current physical register name (PRN) (see Fig 5 Ref 110) there also being stored PRNs previously assigned to the LRN (see Fig 5 Ref 122), and a control circuit that copies the current PRN to another storage location when a new PRN is assigned to a first LRN (see

Fig 5 and Col 15 Line 20 to Col 16 Line 38). Clift et al. teaches register renaming with a history buffer that stores the previous register aliases. The system of Clift et al. reads upon the claimed invention.

B) As to claim 3, the mapper circuit can revert the current PRN to a previous PRN (see Col 7 Lines 18-32).

C) As to claims 4, 5, 7, and 8, it is inherent that the mapper circuit would receive a plurality of control signals, including ones that causes the reverting and ones that cause the "other storage locations" of the mapper circuit to store a copy of a PRN. These control signals would come from the scheduler of the microprocessor when a decision has been made as to whether the instructions executed were the proper ones or a miss speculation has occurred. The "backup indication" can be referred to as any name, including a "insert pointer" - the end result is the same for both the claimed invention and that of Clift et al. A previous register aliasing is restored.

D) As to claim 9, the mapper circuit does have a read port that allows the mappings from the LRN to the PRN to be read, otherwise the data stored in the mapper circuit could never be used.

Claim Rejections – 35 USC § 103

5. The following is a quotation of 35 U.S.C. § 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 10-17 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Clift et al., U.S. Patent 6,633,970, in view of Buti, U.S. Patent 6,421,758.

A) As to claims 10 and 11, Clift et al. discloses the invention as claimed. There is a mapper circuit that provides associations between logical registers and physical registers (see Abstract, Fig 2-5), the mapper circuit comprising a memory that has a plurality of addressable units addressed by different logical register names (LRN) that stores a current physical register name (PRN) (see Fig 5 Ref 110) and a plurality of valid indications (see Fig 5 Ref 316). However, Clift et al. does not disclose that the memory for the mapper is implemented in a content addressable memory. Buti teaches the use of content addressable memory for register renaming (se Col 1 Lines 45-60). The use of CAM provides for the compare logic to match when a LRN is input into the CAM and outputs the PRN that corresponds to that LRN. Accordingly, it would have been obvious to one having ordinary skill in the art at the time the invention was made that a CAM could be utilized for the mapper circuit memory as Buti teaches.

B) As to claim 12, Clift et al. teaches the use of pointers in the history buffer (see Fig 5 Ref 324, 322, and 320).

C) As to claim 13, the mapper circuit does have a write port that allows the mappings from the LRN to the PRN to be written, otherwise the data stored in the mapper circuit could never be updated.

D) As to claim 14-17, Clift et al. discusses the updating and resetting of the "valid bits" when an LRN is assigned a new PRN at different "checkpoints" (see description of Fig 5-8 with regard to Ref 316).

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kevin L. Ellis whose telephone number is 571-272-4205. The examiner can normally be reached on weekdays from 6:00AM-2:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on 571-272-4210. The fax phone numbers for the organization where this application or proceeding is assigned is 571-273-8300.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.

Kevin L. Ellis
Primary Examiner
September 9, 2005